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Course: CIS 310

Professor: Probir Roy

Assignment 3: Integrating the Complete Processor

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**Github Repository:** [**jeevaelango-soccer/Assignment-3**](https://github.com/jeevaelango-soccer/Assignment-3)

**2.3 & 2.4 Extended Instruction Register (IRs) and Instruction Decoder**

**Overview/Description:**

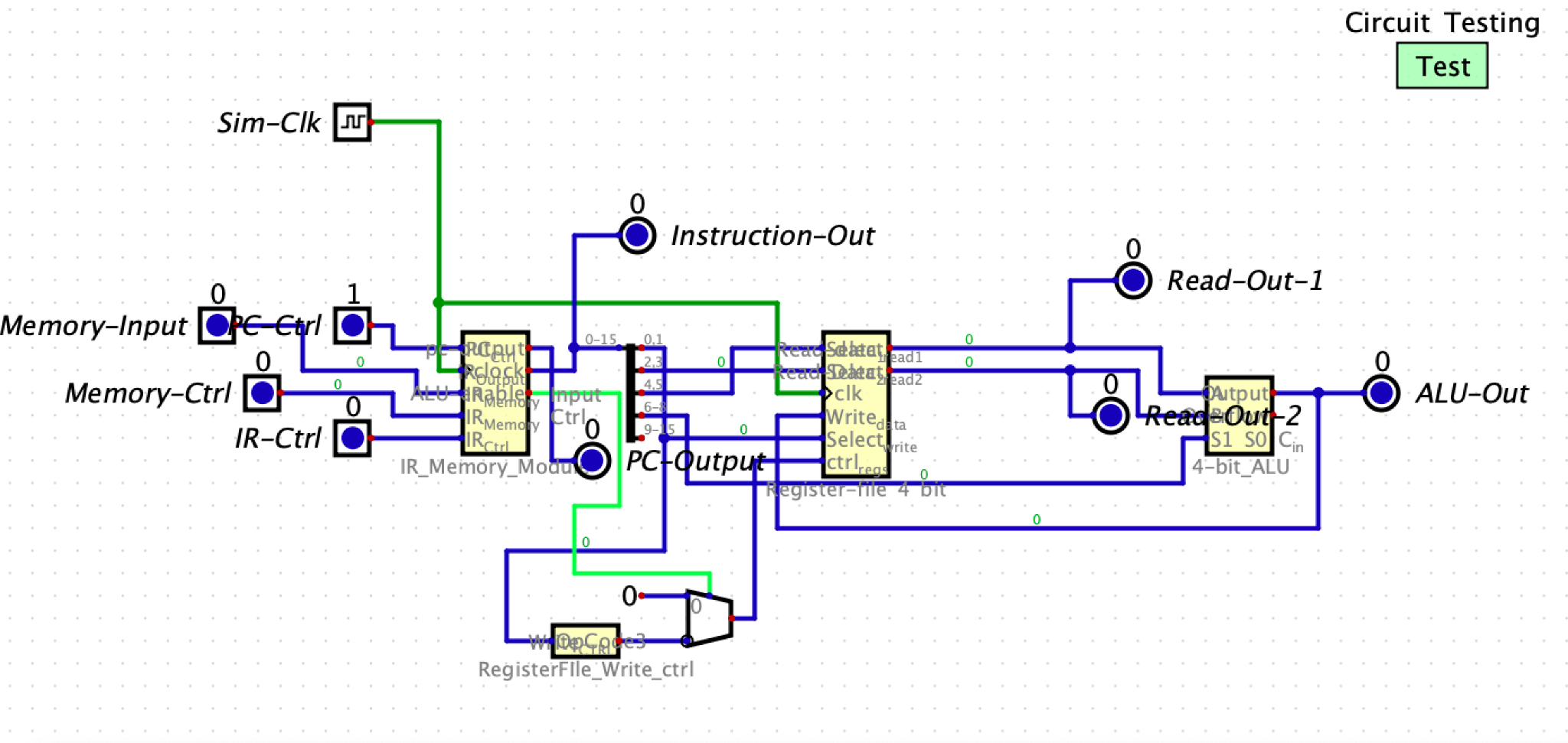
* This is the implementation of the Instruction Register. Its purpose is for the control signal to store data into each IR. The Output is connected to the Register File to be able to read the data and to decide which bit to output. The ALU enable goes to the register write file to the multiplexer and then to the control register in the register file.

**Testing Explanation:**

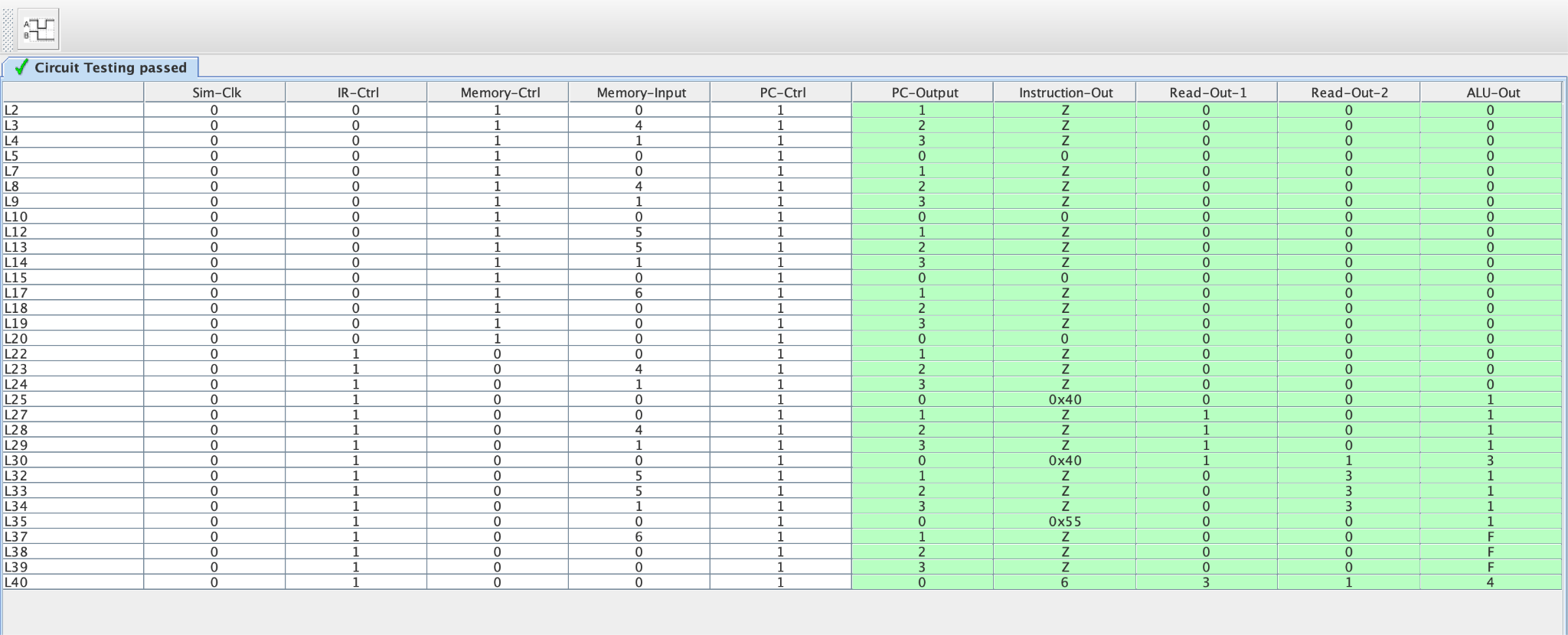
* Extended Instruction Register : There is one input, which is the memory input. There are three outputs, which are read out 1, read out 2, alu out. The way it outputs is by clicking on the clock for sixteen times, for every four cycles, The PC output will go from 1 to 3. The ALU will first output 0, then it will output 1, and then Z, and back to 0\
* Instruction Decoder: There are 3 outputs to test the register file, R-register being input 1, M-Register being input 2, and LM-Register being input 3. The PC output will increment 4 times. For every four cycles, the output for each Instruction memory memory will be 1, and the other four cycles, it will output Z.

**Testing:**

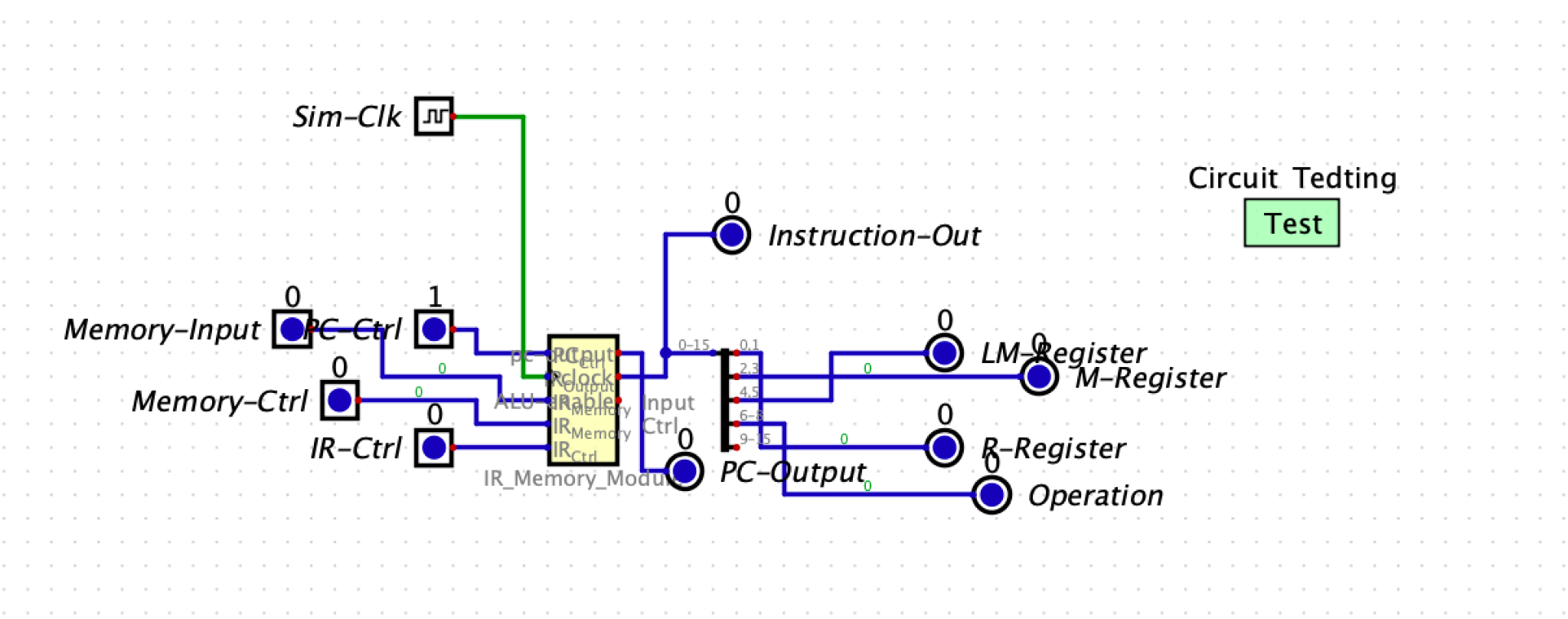
* **Extended Instruction Register**

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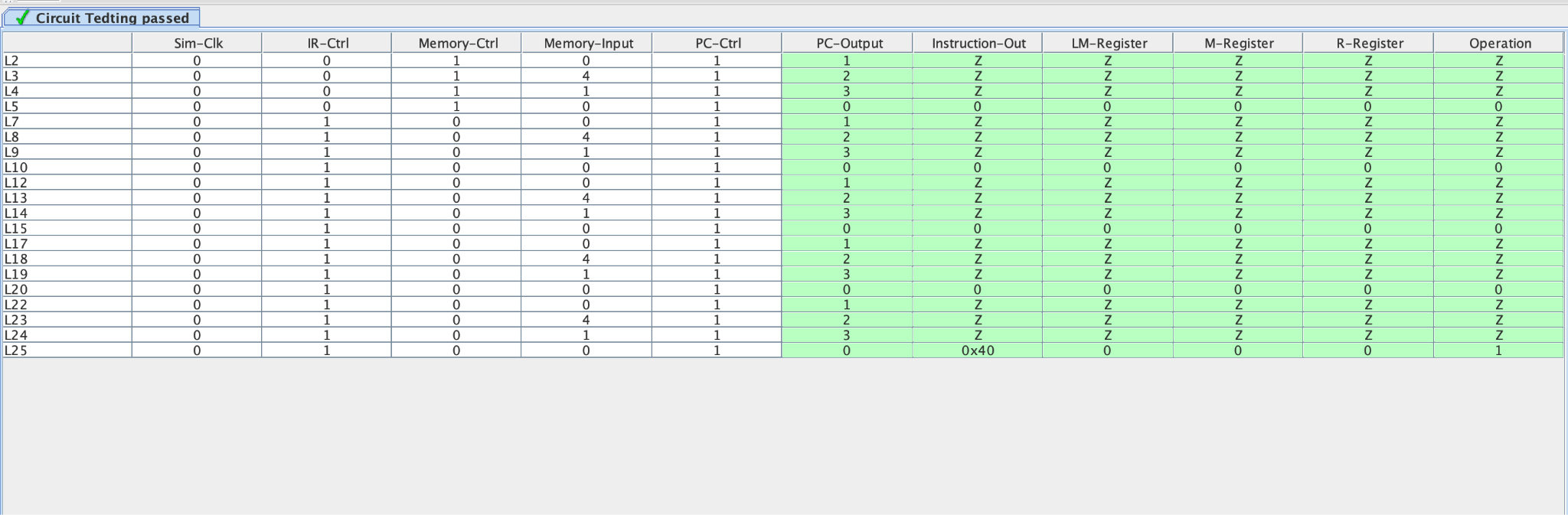
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* Test Decode

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